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EXAMINER
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ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

		Application No.	**Applicant(s)**
		09/849,658	HENRY ET AL.
Office Action Summary		**Examiner**	**Art Unit**	
		Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>04 April 2005</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-63</u> is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-63</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
   application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on
> sale in this country, more than one year prior to the date of application for patent in the United States.

2.   Claims 1-6, 10-33, 36-53, 57-63 are rejected under 35 U.S.C. 102(b) as being clearly

anticipated by Hoyt et al., US Patent 5,604,877.

3.   Referring to claim 1, Hoyt et al. have taught an apparatus in a microprocessor for

detecting that the microprocessor erroneously branched to a speculative target address that is

provided by a branch target address cache (BTAC), the apparatus comprising:

        a.   a storage element, for storing an indication of whether the microprocessor

branched to the speculative target address provided by the BTAC without knowing

whether an instruction associated with said indication is a branch instruction (abstract.

Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65, marked as

predicted or not);

        b.   instruction decode logic, configured to receive and decode said instruction

subsequent to the microprocessor branching to the speculative target address (Figure 5,

element 60, abstract, column 8, lines 25-65, column 12, line 55-column 13, line 65); and

        c.   prediction check logic, coupled to said instruction decode logic, for notifying

branch control logic that the microprocessor erroneously branched to the speculative

target address if said instruction decode logic indicates said instruction is not a branch

instruction and said indication indicates the microprocessor branched to the speculative

target address (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13,

line 65).

4.   Referring to claim 2, Hoyt et al. have taught the apparatus of claim 1, as described above,

and wherein said storage element is in an instruction buffer for storing instructions, including

said instruction (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line

65).

5.   Referring to claim 3 Hoyt et al. have taught the apparatus of claim 1, as described above,

and wherein said indication indicates that the microprocessor branched to the speculative target

address cached in the BTAC without certainty that said instruction decoded by said instruction

decode logic is a same instruction for which the BTAC cached the speculative target address

(abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

6.   Referring to claim 4, Hoyt et al. have taught the apparatus of claim 1, as described above,

and wherein said indication indicates that the microprocessor branched to the speculative target

address provided by the BTAC in response to a fetch address that selected a line of instructions

in an instruction cache (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13,

line 65).

7.   Referring to claim 5, Hoyt et al. have taught the apparatus of claim 4, wherein said

indication indicates that the microprocessor branched to the speculative target address in

response to said fetch address without certainty whether a previously executed instruction, for

which the BTAC cached said target address, is present in said instruction cache line (abstract.

Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

8.   Referring to claim 6 Hoyt et al. have taught the apparatus of claim 1, as described above,

and wherein said instruction decode logic is configured to determine a first instruction length of

said instruction (Inherent, in order to decode the instruction, the decode logic must inherently

determine the length of the instruction.).

9.   Referring to claim 10, Hoyt et al. have taught the apparatus of claim 1, as described

above, and wherein the apparatus further comprises:

    a.   address generation logic, coupled to said instruction decode logic, for generating a

    correct target address of said instruction (abstract. Figure 5, column 8, lines 25-65,

    column 12, line 55-column 13, line 65); and

    b.   a comparator, coupled to said address generation logic, for comparing the

    speculative target address provided by the BTAC and said correct target address of said

    instruction, and for providing a mismatch indicator to said prediction check logic based

    on said comparing (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column

    13, line 65).

10.   Referring to claim 11, Hoyt al. have taught the apparatus of claim 10, as described above,

and wherein said prediction check logic is configured to notify said branch control logic that the

microprocessor erroneously branched to the speculative target address if said mismatch indicator

indicates the speculative target address and said correct target address of said instruction do not

match (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

11.   Referring to claim 12, Hoyt et al. have taught the apparatus of claim 1, as described

above, and wherein the apparatus further comprises: execution logic, operatively coupled to said

instruction decode logic, for determining a correct direction of said instruction, said correct

direction specifying whether said instruction is taken or not taken, said execution logic providing said correct direction to said prediction check logic (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

12.   Referring to claim 13, Hoyt et al. have taught the apparatus of claim 12, as described above, and wherein said prediction check logic is configured to notify said branch control logic that the microprocessor erroneously branched to the speculative target address if said correct direction indicates said instruction is not taken (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

13.   Referring to claim 14, Hoyt et al. have taught an apparatus in a microprocessor for detecting that the microprocessor erroneously speculatively branched to a target address that is provided by a speculative branch target address cache (BTAC), the apparatus comprising:

   a.   a storage element, for storing an indication of whether the microprocessor speculatively branched to the target address provided by the BTAC based on an instruction cache fetch address without first determining whether a branch instruction is present in a line of instruction bytes in the instruction cache selected by said fetch address (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65);

   b.   instruction decode logic, configured to receive and decode said instruction bytes in said instruction cache line subsequent to the microprocessor speculatively branching to the target address, said instruction decode logic further configured to indicate whether said line includes a branch instruction (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65); and

    c.   prediction check logic, coupled to said instruction decode logic, for providing an

error signal to branch control logic if said indication indicates the microprocessor

speculatively branched to the target address and said instruction decode logic indicates

said line does not include a branch instruction (abstract, Figure 5, column 8, lines 25-65,

column 12, line 55-column 13, line 65).

14.   Referring to claim 15, Hoyt et al. have taught the apparatus of claim 14, as described

above, and wherein the target address is provided by a speculative call/return stack in the

microprocessor rather than the speculative BTAC in response to an indication cached in the

BTAC that said line of instruction bytes includes a return instruction (abstract. Figure 5, column

8, lines 25-65, column 12, line 55-column 13, line 65).

15.   Referring to claim16, Hoyt et al. have taught a microprocessor for detecting and

correcting an erroneous speculative branch, comprising:

    a.   an instruction cache, for providing a line of instruction bytes selected by a fetch

address, said fetch address provided to said instruction cache on an address bus (column

5, lines 10-20);

    b.   a speculative branch target address cache (BTAC), coupled to said address bus,

for providing a speculative target address of a previously executed branch instruction in

response to said fetch address whether or not said previously executed branch instruction

is present in said line (Figure 5, element 41, column 8, lines 25-65, column 12, line55-

column 13, line 65);

c.   control logic, coupled to said BTAC, configured to control a multiplexer to select

said speculative target address as said fetch address during a first period (Figure 5,

column 8, lines 25-65, column 12, line 55-column 13, line 65); and

d.   prediction check logic, coupled to said BTAC, configured to detect that said

control logic controlled said multiplexer to select said speculative target address

erroneously because zero branch instructions are present in said line (Figure 5, column 8,

lines 25-65, column 12, line 55-column 13, line 65, No branch instructions present when

a prediction is made.);

e.   wherein said control logic is further configured to control said multiplexer to

select a correct address as said fetch address during a second period in response to said

prediction check logic detecting said erroneous selection (abstract. Figure 5, column 8,

lines 25-65, column 12, line 55-column 13, line 65).

16.   Referring to claim 17, Hoyt et al. have taught the microprocessor of claim 16, as

described above, and wherein said second period is subsequent to said first period (abstract.

Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

17.   Referring to claim 18, Hoyt et al. have taught the microprocessor of claim 16, as

described above, and further comprising: instruction decode logic, configured to receive and

decode said instruction bytes and to specify to said prediction check logic whether a branch

instruction is present in said instruction bytes (Figure 5, element 60, column 12, line 55-column

13, line 65).

18.   Referring to claim 19, Hoyt et al. have taught the microprocessor of claim 18, as

described above, and wherein said prediction check logic detecting that said control logic

controlled said multiplexer to select said speculative target address erroneously comprises said prediction check logic determining that a branch instruction is not present in said instruction bytes (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

19.   Referring to claim 20, Hoyt et al. have taught the microprocessor of claim 16, as described above, and further comprising: branch target address generation logic, configured to receive said line of instruction bytes and to generate an instruction pointer of an instruction comprised in said line of instruction bytes; wherein said correct address comprises said instruction pointer of said instruction (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

20.   Referring to claim 21, Hoyt et al. have taught the microprocessor of claim 20, as described above, and wherein said instruction is comprised in said line of instruction bytes at a location of said previously executed branch instruction in said line (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

21.   Referring to claim 22, Hoyt et al. have taught the microprocessor of claim 21, as described above, and wherein said location is cached in said BTAC (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

22.   Referring to claim 23, Hoyt et al. have taught the microprocessor of claim 16, as described above, and further comprising: branch target address generation logic, configured to receive said line of instruction bytes and to generate a correct branch target address of a branch instruction comprised in said line of instruction bytes based on execution of said branch instruction comprised in said line of instruction bytes; wherein said correct address comprises

said correct branch target address (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

23.   Referring to claim 24, Hoyt et al. have taught the microprocessor of claim 23, as described above, and wherein said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously comprises said prediction check logic determining that said correct branch target address and said speculative target address do not match (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

24.   Referring to claim 25, Hoyt et al. have taught the microprocessor of claim 23, as described above, and wherein said branch instruction is comprised in said line of instruction bytes at a location of said previously executed branch instruction in said line (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

25.   Referring to claim 26, Hoyt et al. have taught the microprocessor of claim 25, and wherein said location is cached in said BTAC (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

26.   Referring to claim 27, Hoyt et al. have taught the microprocessor of claim 16, as described above, and further comprising: execution logic, configured to receive said line of instruction bytes and to generate a correct direction of a branch instruction comprised in said line of instruction bytes, said correct direction generated based on execution of said branch instruction comprised in said line of instruction bytes (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

27.   Referring to claim 28, Hoyt et al. have taught the microprocessor of claim 27, as

described above, and wherein said prediction check logic detecting that said control logic

controlled said multiplexer to select said speculative target address erroneously comprises said

prediction check logic determining that said correct direction indicates said branch instruction

comprised in said line of instruction bytes is not taken (abstract. Figure 5, column 8, lines 25-65,

column 12, line 55-column 13, line 65).

28.   Referring to claim 29, Hoyt et al. have taught the microprocessor of claim 27, as

described above, and wherein said branch instruction is comprised in said line of instruction

bytes at a location of said previously executed branch instruction in said line (abstract. Figure 5,

column 8, lines 25-65, column 12, line 55-column 13, line 65).

29.   Referring to claim 30, Hoyt et al. have taught the microprocessor of claim 29, as

described above, and wherein said location is cached in said BTAC (abstract. Figure 5, column

8, lines 25-65, column 12, line 55-column 13, line 65).

30.   Referring to claim 31, Hoyt et al. have taught the microprocessor of claim 16, as

described above, and further comprising: branch target address generation logic, configured to

receive said line of instruction bytes and to generate an instruction pointer of a next instruction

after an instruction comprised in said line of instruction bytes at a location of said previously

executed branch instruction in said line (abstract. Figure 5, column 8, lines 25-65, column 12,

line 55-column 13, line 65); wherein said correct address comprises said instruction pointer of

said next instruction after said instruction (abstract. Figure 5, column 8, lines 25-65, column 12,

line 55-column 13, line 65).

31.   Referring to claim 32, Hoyt et al. have taught the microprocessor of claim 31, as

described above, and wherein said location is cached in said BTAC (abstract. Figure 5, column

8, lines 25-65, column 12, line 55-column 13, line 65).

32.   Referring to claim 33, Hoyt et al. have taught the microprocessor of claim 16, as

described above, and further comprising:

        a.   instruction decode logic, configured to receive and decode said line of instruction

        bytes and to specify a length of an instruction comprised in said line of instruction bytes,

        said instruction being at a location of said previously executed branch instruction in said

        line (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65,

        Inherent, in order for Hoyt et al. to decode the instruction, the decode logic must

        inherently specify the length of the instruction.).

33.   Referring to claim 36, Hoyt et al. have taught the microprocessor of claim 16, as

described above, and further comprising: instruction decode logic, configured to receive and

decode said instruction and to specify which of a plurality of bytes comprising said instruction is

an opcode byte (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line

65).

34.   Referring to claim 37, Hoyt et al. have taught the microprocessor of claim 36, as

described above, and wherein said prediction check logic detecting that said control logic

controlled said multiplexer to select said speculative target address erroneously comprises said

prediction check logic determining that said control logic controlled said multiplexer to select

said speculative target address based on a byte of said instruction other than said opcode byte

specified by said instruction decode logic (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

35.   Referring to claim 38, Hoyt et al. have taught the microprocessor of claim 16, as described above, and further comprising: branch target address generation logic, configured to receive said line of instruction bytes and to generate an instruction pointer of an instruction comprised in said line of instruction bytes, said instruction located at a location of said previously executed branch instruction in said line; wherein said correct address comprises said instruction pointer of said instruction (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

36.   Referring to claim 39, Hoyt et al. have taught the microprocessor of claim 16, as described above, and wherein an entry of said speculative BTAC caching said speculative target address is invalidated in response to said prediction check logic detecting said erroneous selection (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

37.   Referring to claim 40, Hoyt et al. have taught the microprocessor of claim 16, as described above, and wherein said speculative BTAC is updated with a direction prediction associated with said previously executed branch instruction, said speculative BTAC being updated in response to said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

38.   Referring to claim 41, Hoyt et al. have taught the microprocessor of claim 16, as described above, and wherein said speculative target address is updated in said speculative BTAC in response to said prediction check logic detecting that said control logic controlled said

multiplexer to select said speculative target address erroneously (abstract. Figure 5, column 8,

lines 25-65, column 12, line 55-column 13, line 65).

39.   Referring to claim 42, Hoyt et al. have taught the microprocessor of claim 16, as

described above, and wherein said prediction check logic comprises an error output, coupled to

said control logic, for notifying said control logic of said prediction check logic detecting that

said control logic controlled said multiplexer to select said speculative target address erroneously

(abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13, line 65).

40.   Referring to claim 43, Hoyt et al. have taught the microprocessor of claim 16, as

described above, and wherein a plurality of pipeline stages of the microprocessor are flushed in

response to said prediction check logic detecting that said control logic controlled said

multiplexer to select said speculative target address erroneously (abstract. Figure 5, column 8,

lines 25-65, column 12, line 55-column 13, line 65).

41.   Referring to claim 44, Hoyt et al. have taught the microprocessor of claim 16, as

described above, and further comprising: an instruction buffer, coupled to said instruction cache,

for buffering said line of instruction bytes; wherein said instruction buffer is flushed in response

to said prediction check logic detecting that said control logic controlled said multiplexer to

select said speculative target address erroneously (abstract. Figure 5, column 8, lines 25-65,

column 12, line 55-column 13, line 65).

42.   Referring to claim 45, Hoyt et al. have taught the microprocessor of claim 16, as

described above, and wherein said speculative BTAC and said instruction cache are accessed

substantially in parallel (abstract. Figure 5, column 8, lines 25-65, column 12, line 55-column 13,

line 65).

43.   Claims 46-53, and 57-63 do not recite limitations above the claimed invention set forth in

claims 1-6, 10-15 and are therefore rejected for the same reasons set forth in the rejection of

claims 1-6, 10-15 above.

Claim Rejections - 35 USC § 103

44.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

45.   Claims 7, 34, 35, 54, 55, and 56 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Hoyt et al., US Patent 5,604,877, in view of Fite et al., US Patent 5,142,634.

46.   Referring to claim 7, Hoyt et al. have taught the apparatus of claim 6, as described above.

They have not specifically taught wherein said prediction check logic is configured to notify said

branch control logic that the microprocessor erroneously branched to the speculative target

address if said first instruction length does not match a second instruction length that is cached in

the BTAC and received therefrom. However, Fite et al. have taught prediction check logic is

configured to determine if said first instruction length does not match a second instruction length

that is cached in the BTAC and received therefrom (Fite et al., column 16, line 27-62, column

21, lines 14-15, column 24, lines 9-26, column 27, lines 9-24) for the desirable purpose of

determining whether the address of the branch instructions has a valid associated entry in the

cache. It would have been obvious to one of ordinary skill in the art at the time the invention

was made to have the branch control logic of Hoyt et al. notify said branch control logic that the

microprocessor erroneously branched to the speculative target address, using the instruction

length comparison concept, as taught by Fite et al., for the desirable purpose of determining

branch speculation validity (Fite et al., column 16, line 27-62, column 21, lines 14-15, column

24, lines 9-26, column 27, lines 9-24).

47.   Referring to claim 34, Hoyt et al. have taught the microprocessor of claim 33, as

described above. They have not specifically taught wherein said prediction check logic detecting

that said control logic controlled said multiplexer to select said speculative target address

erroneously comprises said prediction check logic determining that said length of said instruction

does not match an instruction length cached in said speculative BTAC for said previously

executed branch instruction. However, Fite et al. have taught prediction check logic is

configured to determine if said first instruction length does not match a second instruction length

.that is cached in the BTAC and received therefrom (Fite et al., column 16, line 27-62, column

21, lines 14-15, column 24, lines 9-26, column 27, lines 9-24) for the desirable purpose of

determining whether the address of the branch instructions has a valid associated entry in the

cache. It would have been obvious to one of ordinary skill in the art at the time the invention

was made to have the branch control logic of Hoyt et al. notify said branch control logic that the

microprocessor erroneously branched to the speculative target address, using the instruction

length comparison concept, as taught by Fite et al., for the desirable purpose of determining

branch speculation validity (Fite et al., column 16, line 27-62, column 21, lines 14-15, column

24, lines 9-26, column 27, lines 9-24).

48.   Referring to claim 35, Hoyt et al. have taught the microprocessor of claim 34, as

described above, and further comprising: branch target address generation logic, configured to

receive said instruction and to generate an instruction pointer of said instruction; wherein said

correct address comprises said instruction pointer of said instruction (abstract. Figure 5, column

8, lines 25-65, column 12, line 55-column 13, line 65).

49.   Claim 54 does not recite limitations above the claimed invention set forth in claims 1-53

and is therefore rejected for the same reasons set forth in the rejection of claims 1-53 above.

50.   Referring to claim 55, Hoyt et al., in combination with Fite et al. have taught the method

of claim 54, as described above, and further comprising: invalidating an entry containing the

speculative target address in the BTAC if said length of the presumed branch instruction does not

match said instruction length speculatively provided by the branch target address cache (Fite et

al., column 16, line 27-62, column 21, lines 14-15, column 24, lines 9-26, column 27, lines 9-

24).

51.   Referring to claim 56, Hoyt et al., in combination with Fite et al. have taught the method

of claim 55, as described above, and wherein said invalidating is performed prior to said

branching to said instruction pointer (Fite et al., column 16, line 27-62, column 21, lines 14-15,

column 24, lines 9-26, column 27, lines 9-24, Hoyt et al., abstract. Figure 5, column 8, lines 25-

65, column 12, line 55-column 13, line 65).

52.   Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoyt et.,

US Patent 5,604,877, in view of Brown et al., US Patent 5,867,701.

53.   Referring to claim 8, Hoyt et al. have taught the apparatus of claim 1, as described above.

They have not specifically taught wherein said prediction check logic is configured to notify said

branch control logic that the microprocessor erroneously branched to the speculative target

address if said indication is associated with a byte of said instruction not defined as a valid

opcode byte by an instruction set of the microprocessor. However, Brown et al. have taught

prediction check logic is configured to notify said branch control logic that the microprocessor

erroneously branched to the speculative target address if said indication is associated with a byte

of said instruction not defined as a valid opcode byte by an instruction set of the microprocessor

for the desirable purpose of flushing out erroneous instructions to avoid a system fault (Brown et

al., column 10, lines 45-54). It would have been obvious to one of ordinary skill in the art at the

time the invention was made to have the prediction check logic of Hoyt et al. be configured to

notify said branch control logic that the microprocessor erroneously branched to the speculative

target address if said indication is associated with a byte of said instruction not defined as a valid

opcode byte by an instruction set of the microprocessor, as taught by Brown et al., for the

desirable purpose of flushing out erroneous instructions to avoid a system fault (Brown et al.,

column 10, lines 45-54).

54.   Referring to claim 9, Hoyt et al. have taught the apparatus of claim 8, as described above.

Hoyt et al. have not specifically taught wherein said microprocessor instruction set is an x86

architecture instruction set. However, it would have been obvious to on of ordinary skill in the

art at the time the invention was made to have the instruction set be an x86 instruction set since

they are among the most commonly used instruction sets in the industry. Official Notice has

been taken.

Response to Arguments

55.   Applicant's arguments with respect to claims 1-63 have been considered but are moot in

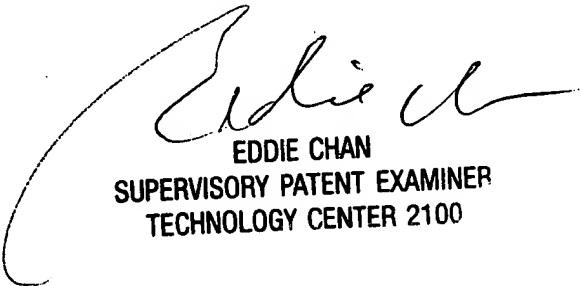view of the new ground(s) of rejection.

Conclusion

56.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170.

The examiner can normally be reached on Monday-Friday, 8-4:30.

57.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

58.   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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SUPERVISORY PATENT EXAMINER
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